

AMENDMENT TO THE CLAIMS

The following listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-37. (canceled)

38. (original) A packet recording apparatus comprising:

arrival time control clock generating means for generating arrival time control clocks in synchronism with input of a time reference value added to input packets;

arrival time identification reference value generating means for generating arrival time identification reference values in synchronism with the arrival time control clocks generated by said arrival time control clock generating means;

synchronization determining means for determining whether the arrival time control clocks are synchronous with the input of the time reference value or not, said synchronization determining means providing a first signal when the arrival time control clocks are synchronous with the input of the time reference value and a second signal when the arrival time control clocks are asynchronous with the input of the time reference value;

adding means for adding the arrival time identification reference values to the input packets;

switching means for switching between a first operation and a second operation, the first operation being provided in response to the first signal from said synchronization determining means to allow operations of said arrival time control clock

generating means and said adding means, the second operation being provided in response to the second signal from said synchronization determining means to inhibit the operation of said arrival time control clock generating means; and

recording means for recording the packets to which the arrival time identification reference values are added by said adding means on a storage medium.

39. (original) A packet recording apparatus as set forth in claim 38, wherein said arrival time control clock generating means includes an extracting circuit which extracts the time reference value from the packets and a feedback loop comparing a count value provided by a counter based on the time reference value with the time reference value to determine a difference therebetween to control a frequency of oscillations provided by an oscillator according to said difference to output the oscillations as said arrival time control clocks and to feedback the oscillations to the counter as being used as the time reference value in following cycles, and wherein said synchronization determining means includes an averaging circuit which averages the differences derived by arrival time control clock generating means for given number of cycles and a comparing circuit which compares an output signal from said averaging means with a given reference value to provide the first and second signals based on a result of the comparison.

40. (original) A packet recording apparatus comprising:

arrival time control clock generating means for generating arrival time control clocks in synchronism with input of a time reference value added to input packets;

arrival time identification reference value generating means for generating arrival time identification reference values in synchronism with the arrival time control clocks generated by said arrival time control clock generating means;

lock flag producing means for producing a lock flag indicative of a synchronization condition of said arrival time control clock generating means a preselected period of time after a first one of the packets is inputted to said arrival time control clock generating means;

adding means for adding the lock flag along with the arrival time identification reference values to the input packets; and

recording means for recording the packets to which the arrival time identification reference values are added by said adding means on a storage medium.

41. (original) A packet recording apparatus comprising:

arrival time control clock generating means for generating arrival time control clocks in synchronism with input of a time reference value added to input packets;

arrival time identification reference value generating means for generating arrival time identification reference values in synchronism with the arrival time control clocks generated by said arrival time control clock generating means;

synchronization determining means for determining whether the arrival time control clocks are synchronous with the input of the time reference value or not, said synchronization determining means providing a first signal when the arrival time control clocks are synchronous with the input of the time reference value and a second signal

when the arrival time control clocks are asynchronous with the input of the time reference value;

adding means for adding the arrival time identification reference values to the input packets;

recording means for recording the packets to which the arrival time identification reference values are added by said adding means on a storage medium; and

controlling means for controlling an operation of said recording means, said controlling means supplying the packets to said adding means at all times, activating the operation of said recording means in response to the first signal from said synchronization determining means, and deactivating the operation of said recording means in response to the second signal from said synchronization determining means.

42. (original) A packet recording apparatus as set forth in claim 38, wherein said packets are transmitted by digital signals carrying one or more programs and said time reference value added to one of said packets.

43. (original) A packet recording apparatus as set forth in claim 40, wherein said packets are transmitted by digital signals carrying one or more programs and said time reference value added to one of said packets.

44. (original) A packet recording apparatus as set forth in claim 41, wherein said

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packets are transmitted by digital signals carrying one or more programs and said time reference value added to one of said packets.

45-47. (canceled)